APPEAL BRIEF UNDER 37 C.F.R. § 41.37

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Arup Bhattacharyya	Examiner: Thomas L. Dickey
Serial No.: 10/612,793	Group Art Unit: 2826
Filed: July 02, 2003	Docket: 1303.111US1

For: HIGH-PERFORMANCE ONE-TRANSISTOR MEMORY CELL

APPEAL BRIEF UNDER 37 CFR § 41.37

Mail Stop Appeal Brief- Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The Appeal Brief is presented in support of the Notice of Appeal to the Board of Patent Appeals and Interferences, filed on February 12, 2009, from the Final Rejection of claims 1-4, 6-7, 20-21, 25-26, 32-34, 37, 39, 63-65, 67, 69, 71-74 and 77 of the above-identified application, as set forth in the Final Office Action mailed on February 10, 2009.

The Commissioner of Patents and Trademarks is hereby authorized to charge Deposit Account No. 19-0743 in the amount of $540.00 which represents the requisite fee set forth in 37 C.F.R. § 41.20(b)(2). The Appellants respectfully request consideration and reversal of the Examiner's rejections of pending claims.

1. REAL PARTY IN INTEREST

The real party in interest of the above-captioned patent application is the assignee, MICRON TECHNOLOGY, INC..

2. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellant that will have a bearing on the Board's decision in the present appeal.

3. STATUS OF THE CLAIMS

Claims 1-79 are pending.

Claims 80-100 were canceled during prosecution as being drawn to a non-elected group of claims.

Claims 5, 8-19, 22-24, 27-31, 35, 36, 38, 40-62, 66, 68, 70, 75, 76, 78 and 79 have been withdrawn by the Examiner.

Claims 1-4, 6, 7, 20, 21, 25, 26, 32-34, 37, 39, 63-65, 67, 69, 71-74 and 77 stand rejected.

Claims 1-4, 6, 7, 20, 21, 25, 26, 32-34, 37, 39, 63-65, 67, 69, 71-74 and 77 are being appealed.

4. STATUS OF AMENDMENTS

No amendments have been made subsequent to the Final Office Action dated February 3, 2009.

5. SUMMARY OF CLAIMED SUBJECT MATTER

The following summary does not provide an exhaustive or exclusive view of the claimed subject matter, and Appellant refers to the appended claims for a complete statement of the claimed subject matter. References to the specification and drawings of the application are provided as examples, and are not intended to indicate that these references are the only references from the specification and drawings that can be applied to the claims.

INDEPENDENT CLAIM 1

Claim 1 recites a memory cell, such as 100, 200, 300, 400, 500, 600 as illustrated in FIGS. 1A-1B, 2A-2B, 3A-3B, 4A-4B, 5A-5B and 6A. With reference to page 8 line 8 to page 20 line 16, the recited memory cell includes an access transistor 101, 201, 301, 401, 501, 601 and a diode 102, 202, 302, 402, 502, 602. The access transistor has a floating node 106, 206, 306, 406, 506, 606 to store a charge indicative of a memory state of the memory cell. The diode exhibits Negative Differential Resistance (NDR) behavior (see, for example, page 8 lines 23-27 and page 11 lines 18-25). The diode is connected between the floating node and a diode reference potential line V_{REF}. The diode includes an anode 104, 204, 304, 404, 504, a cathode 103, 203, 303, 403, 503 and an intrinsic region (i) between the anode and the cathode. The intrinsic region of the diode assists with stabilizing the memory state of the memory cell (see, fore example, page 8 line 12 to page 9 line 1). The diode has a structure to allow the memory cell to switch memory states (see, for example, page 10 line 23-25) using a forward or reverse bias voltage (see, for example, page 11 lines 20-25) across the diode without gating the diode (see for example, page 9 lines 2-4 and lines 22-23).

INDEPENDENT CLAIM 6

Claim 6 recites a memory cell, such as 100, 200, 300, 400, 500, 600 as illustrated in FIGS. 1A-1B, 2A-2B, 3A-3B, 4A-4B, 5A-5B and 6A. With reference to page 8 line 8 to page 20 line 16, the recited memory cell includes an access transistor 101, 201, 301, 401, 501, 601 and a Negative Differential Resistance (NDR) diode 102, 202, 302, 402, 502, 602. The access transistor has a first diffusion region 105, 605 connected to a bit line (BL), and a second

diffusion region 106, 606 to store a charge indicative of a memory state of the memory cell (see, for example, page 8 lines 12-13). The NDR diode is connected between the second diffusion region and a diode reference potential line V_{REF}. The diode includes an anode 104, 204, 304, 404, 504, a cathode 103, 203, 303, 403, 503, an intrinsic region (i) between the anode and cathode to assist with stabilizing the memory state of the memory cell (see, for example, page 8 line 12 to page 9 line 1), and a diode gate 110, 210, 310, 410, 510, 610 operatively positioned with respect to the intrinsic region to enhance switching performance between memory states (see, for example, page 9 lines 7-15 and 20-21). The diode has a structure to allow the memory cell to switch memory states (see, for example, page 10 line 23-25) using a forward or reverse bias voltage (see, for example, page 11 lines 20-25) across the diode without gating the diode (see for example, page 9 lines 2-4 and lines 22-23). The memory cell is adapted to gate the gate-controlled diode to enhance switching between memory states (see for example, page 9 lines 7-15 and lines 20-21).

INDEPENDENT CLAIM 7

Claim 7 recites a memory cell, such as 200 and 600 as illustrated in FIGS. 2A-2B and 6A. With reference to page 8 line 8 to page 12 line 26 and page 15 line 5 to page 20 line 16, the recited memory cell includes an n-channel access transistor 201, 601 and a Negative Differential Resistance (NDR) n/i/p diode 202, 602. The transistor is on a bulk semiconductor substrate 611. The n-channel access transistor has a first n-type diffusion region 605 connected to a bit line (BL) and a second n-type diffusion region 606 to store a charge indicative of a memory state of the memory cell (see, for example, page 8 lines 12-13). The diode has an n-type anode 204 connected to a diode reference potential line V_{REF}, a p-type cathode 203 in contact with the second n-type diffusion region, and an intrinsic region (i) between the anode and the cathode to assist with stabilizing the memory state of the memory cell (see, for example, page 8 line 12 to page 9 line 1). The diode has a structure to allow the memory cell to switch memory states (see, for example, page 10 line 23-25) using a forward or reverse bias voltage (see, for example, page 11 lines 20-25) across the diode without gating the diode (see for example, page 9 lines 2-4 and lines 22-23).

INDEPENDENT CLAIM 20

Claim 20 recites a memory cell, such as such as 100, 200, 300, 400, 500, 600 as illustrated in FIGS. 1A-1B, 2A-2B, 3A-3B, 4A-4B, 5A-5B and 6A. With reference to page 8 line 8 to page 20 line 16, the recited memory cell includes an access transistor 101, 201, 301, 401, 501, 601 and a Negative Differential Resistance (NDR) diode 102, 202, 302, 402, 502, 602. The access transistor includes a body region 107, 612, a first diffusion region 105, 605 electrically connected to a bit line (BL), a second diffusion region 106, 606 separated from the first diffusion region by a channel area 613 in the body region, and a gate 108, 608 separated from the channel area by a gate insulator 109, 609. The gate is electrically connected to a word line (WL1). The NDR diode includes an anode 104, 204, 304, 404, 504, a cathode 103, 203, 303, 403, 503, and an intrinsic region (i) between the anode and the cathode. The diode is connected between the second diffusion region and a diode reference potential line. The diode has a structure to allow the memory cell to switch memory states (see, for example, page 10 line 23-25) using a forward or reverse bias voltage (see, for example, page 11 lines 20-25) across the diode without gating the diode (see for example, page 9 lines 2-4 and lines 22-23). The memory cell is operative to store and sense a charge in the second diffusion region that is representative of a memory state.

INDEPENDENT CLAIM 33

Claim 33 recites a memory cell, such as100, 200, 300, 400, 500, 600 as illustrated in FIGS. 1B, 2B, 3B, 4B, 5B and 6A. With reference to page 8 line 8 to page 20 line 16, the recited memory cell includes an access transistor 101, 201, 301, 401, 501, 601 and a gate-controlled Negative Differential Resistance (NDR) diode 102, 202, 302, 402, 502, 602. The access transistor is formed in a bulk semiconductor structure 611. The access transistor includes a first diffusion region 105, 605 separated from a second diffusion region 106, 606 by a channel region 613, and further includes a gate 108, 608 separated from the channel region by a gate insulator 109, 609. The first diffusion region is connected to a bit line (BL) and the gate is connected to a first word line (WL1). The gate-controlled NDR diode is connected between a reference potential line V_{REF} and the second diffusion region. The diode includes an anode 104, 204, 304, 404, 504 a cathode 103, 203, 303, 403, 503, an intrinsic region (i) positioned between the anode

and the cathode, and a diode gate 110, 210, 310, 410, 510 610 operably positioned with respect to the intrinsic region. The diode gate is connected to a second word line (WL2). The diode has a structure to allow the memory cell to switch memory states (see, for example, page 10 line 23-25) using a forward or reverse bias voltage (see, for example, page 11 lines 20-25) across the diode without gating the diode (see for example, page 9 lines 2-4 and lines 22-23). The memory cell is adapted to gate the gate-controlled diode to enhance switching between memory states (see, for example, page 9 lines 2-25).

INDEPENDENT CLAIM 63

Claim 63 recites a memory cell, such as 100, 200, 400, 600 as illustrated in FIGS. 1A-1B, 2A-2B, 4A-B, and 6A. With reference to page 8 line 8 to page 20 line 16, the recited memory cell includes an access transistor 101, 201, 401, 601 and a Negative Differential Resistance (NDR) n/i/p diode 102, 202, 402, 602. The access transistor includes a first diffusion region 105, 605 separated from a second diffusion region 106, 606 by a channel region 613, and further includes a gate 108, 608 separated from the channel region by a gate insulator 109, 609. The first diffusion region is connected to a bit line (BL) and the gate is connected to a first word line (WL1). The NDR n/i/p diode is connected between a diode reference potential line V_{REF} and the second diffusion region. The n/i/p diode includes an n-type anode 104, 204, 404, a p-type cathode 103, 203, 403, and an intrinsic region (i) positioned between the anode and the cathode, The diode has a structure to allow the memory cell to switch memory states (see, for example, page 10 line 23-25) using a forward or reverse bias voltage (see, for example, page 11 lines 20-25) across the diode without gating the diode (see for example, page 9 lines 2-4 and lines 22-23).

INDEPENDENT CLAIM 72

Claim 72 recites a memory device, such as 2550 as illustrated in FIG.25 (see also FIGS. 1A-B, 2A-2B, 3A-3B, 4A-4B, 5A-5B, 6A-6B). With reference to page 46 lines 6-24, the recited memory device includes a memory array 2551, a number of word lines 2555, a number of bit lines 2556, at least one reference line V_{REF} and control circuitry 2552. The memory array includes a plurality of memory cells 2554 in rows and columns. Each word line is connected to a row of memory cells. Each bit line connected to a column of memory cells. The at least one

reference line provides a reference potential to the memory cells. The control circuitry includes word line select circuitry 2557 and bit line select circuitry 2558 to select a number of memory cells for writing and reading operations. Each memory cell 2554, 100, 200, 300, 400, 500, 600 includes an access transistor 101, 201, 301, 401, 501, 601 and a Negative Differential Resistance (NDR) diode 102, 202, 302, 402, 502, 602. The access transistor includes a body region 107, 612, a first diffusion region 105, 605 electrically connected to one of the bit lines, a second diffusion region 106, 606 separated from the first diffusion region by a channel area 613 in the body region, and a gate 108, 608 separated from the channel area by a gate insulator 109, 609 and electrically connected to one of the word lines. The NDR diode includes an anode 104, 204, 304, 404, 504, a cathode 103, 203, 403, 503, and an intrinsic region (i) between the anode and the cathode. The diode is connected between the second diffusion region and a diode reference line. The diode has a structure to allow the memory cell to switch memory states (see, for example, page 10 line 23-25) using a forward or reverse bias voltage (see, for example, page 11 lines 20-25) across the diode without gating the diode (see for example, page 9 lines 2-4 and lines 22-23). The memory cell is adapted to store a charge in the second diffusion region of the access transistor to indicate a stable memory state.

This summary does not provide an exhaustive or exclusive view of the present subject matter, and Appellant refers to each of the appended claims and its legal equivalents for a complete statement of the invention.

6. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Whether claims 1-4, 6, 7, 20, 21, 25, 26, 32-34, 37, 39, 63-65, 67, 69, 71-74 and 77 were properly rejected under 35 U.S.C. §103(a) as being unpatentable over NEMATI ET AL. (6,229,161) in view of KRIVOKAPIC (6,291,832).

7. ARGUMENT

A) The Applicable Law

The question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art, (2) any differences between the claimed subject matter and the prior art, (3) the level of skill in the art. *Graham v. John Deere Co.,* 383 U.S. 1, 17-18, 148 USPQ 459, 467 (1966). *See also KSR Int'l Co. v. Teleflex Inc.,*, 127 S.Ct 1727, 1734, 82 USPQ2d 1385, 1391 (2007) (While the sequence of these questions might be reordered in any particular case, the [*Graham]* factors continue to define the inquiry that controls).

The Supreme Court stated "[o]ften, it will be necessary for a court to look to interrelated teachings of multiple patents; the effects of demands known to the design community or present in the marketplace; and the background knowledge possessed by a person having ordinary skill in the art, all in order to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue." *Id.* at 1740-41, 82 USPQ2d at 1396. The Court noted that "[t]o facilitate review, this analysis should be made explicit. *Id.* (citing *In re Kahn,* 441 F.3d 977, 988, 78 USPQ2d 1329, 1336 (Fed. Cir. 2006)). ("[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness."). *Id* at 1741, 82 USPQ2d at 1396.

"All words in a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970)." *MPEP 2144.03* states, with respect to rejections taking official notice of facts not in the record, "such rejections should be judiciously applied." Section A of this MPEP section states: "It would not be appropriate for the examiner to take official notice of facts without citing a prior art reference where the facts asserted to be well known are not capable of instant and unquestionable demonstration as being well-known." Section B of this MPEP section indicates that, if official notice is taken of a fact, unsupported by documentary evidence, the technical line of reasoning underlying a decision to take such notice must be clear and unmistakable.

According to MPEP 706.02(j), the following should be set forth in a §103 rejection: (A)

the relevant teachings of the prior art relied upon, preferably with reference to the relevant column or page number(s) and line number(s) where appropriate; (B) the difference or differences in the claim over the applied reference(s); (C) the proposed modification of the applied reference(s) necessary to arrive at the claimed subject matter; and (D) an explanation why one of ordinary skill in the art at the time the invention was made would have been motivated to make the proposed modification. Additionally, this section states that it is important for an examiner to properly communicate the basis for a rejection so that the issues can be identified early and the applicant can be given fair opportunity to reply.

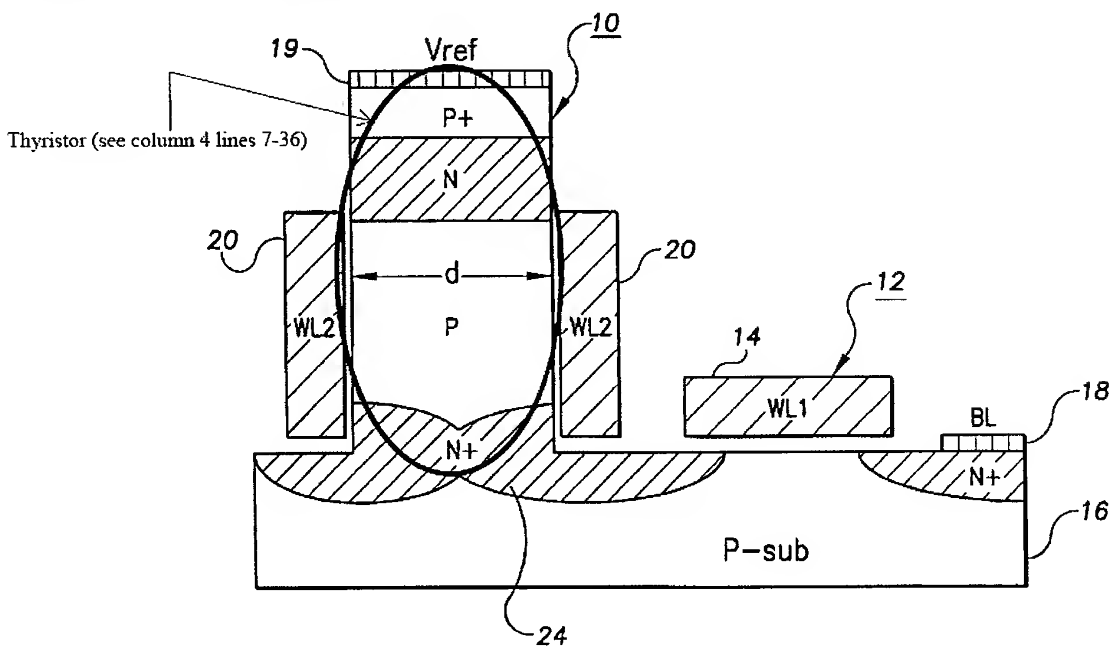
A functional limitation must be evaluated and considered, just like any other limitation of the claim, for what it fairly conveys to a person of ordinary skill in the pertinent art in the context in which it is used. MPEP § 2173.05(g). Limitations such as "members adapted to be positioned" serve to precisely define present structural attributes of interrelated component parts of the claimed assembly. *In re Venezia*, 530 F.2d 956, 189 USPQ 149 (CCPA 1976).

B) Discussion of the rejection of claims 1-4, 6, 7, 20, 21, 25, 26, 32-34, 37, 39, 63-65, 67, 69, 71-74 and 77 under 35 U.S.C. §103(a) as being unpatentable over NEMATI ET AL. (6,229,161) in view of KRIVOKAPIC (6,291,832).

<u>The Nemati et al. Reference</u>

An example of the thyristor of Nemati et al. is illustrated in FIG. 1. Nemati et al. indicate that the structure can be used for SRAM cells (Abstract, col. 4 lines 11-12). Nemati et al. use multiple PN structures (col. 3 line 52). Nemati et al indicate that there are different NDR devices and that these different NDR devices have different basis for operation such as a bipolar transistor and quantum-effect devices (col. 3 lines 51 to col. 2 line 26); and Nemati et al. further indicate that thyristors are used for power switching (col. 2 lines 13-26, 58-61).

FIG. 1 **Nemati et al.**



The Krivokapic Reference

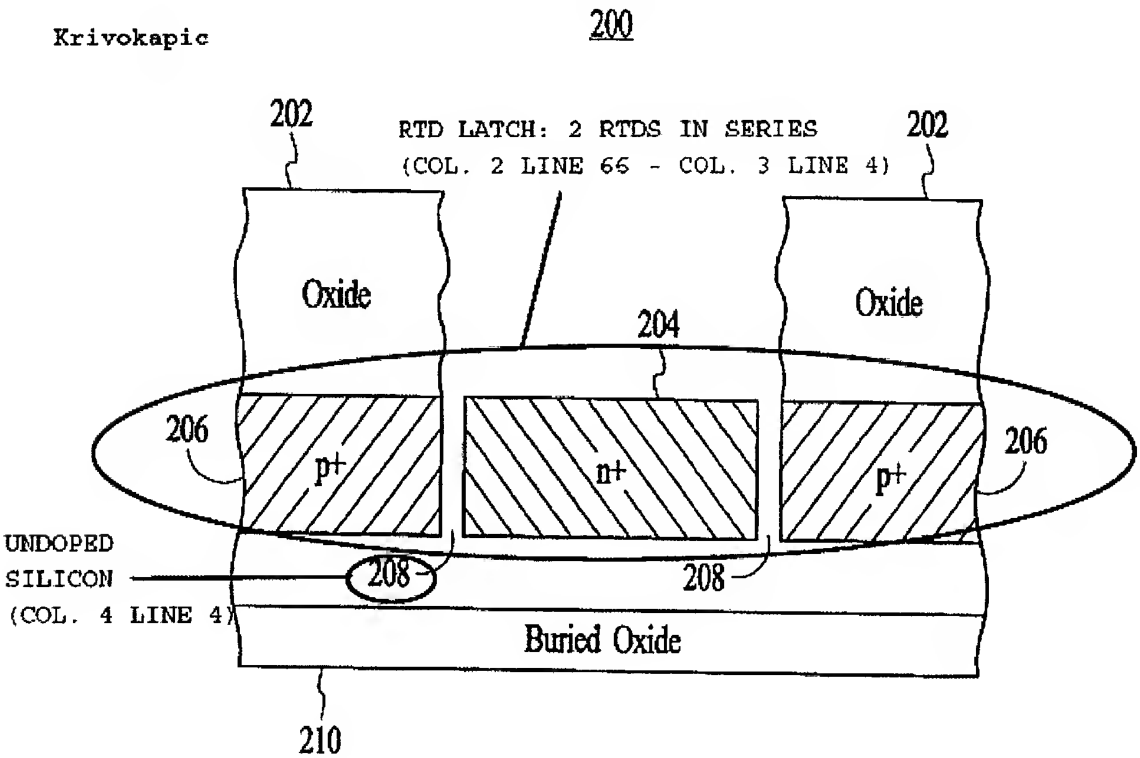


FIG. 5

The Krivokapic reference was cited for the first time by the Office in the Final Office Action. Krivokapic refers to a resonant tunneling diode (RTD) latch (title, col. 2 lines 52-53). The latch comprises two diodes in series (col. 2 line 66 to col. 3 line 4). RTDs have high speed applications for CMOS designs (col. 1 lines 31-32). Portions of the current-voltage curves exhibit negative differential resistance (col. 1 lines 34-35). The tunneling occurs through a potential barrier having a very narrow width (col. 1 line 36).

Krivokapic does not describe the resonant tunneling in an RTD. Appellant respectfully submits that the quantum well thickness and the barrier thickness for an RTD are important parameters (resonant tunneling occurs if they are sufficiently small). If these parameters are appropriately small, a set of discrete barrier energy levels exist inside the well, and an incident electrode tunnels through the double barrier with a unity (100%) transmission coefficient when the incident electron has an energy that exactly equal one of the discrete energy levels inside the well.

The Rejection

The Office improperly asserts that the person of ordinary skill in the art is (a) a person with a level of skill that is "extremely high" (Final Office Action at page 9 line 18) and (b) a person with "extraordinary creativity" (Final Office Action at page 10 lines 7-8).

It is acknowledged that one of ordinary skill in the semiconductor art will be educated. However, the Office is incorrect to assert that the standard for semiconductor technology is "extremely high" skill and "extraordinary creativity" for the semiconductor technology. Further, it is improper for the Office to postulate that the Supreme Court "might easily have said that in the semiconductor art the person of ordinary skill is a person of <u>extraordinary</u> creativity" (Final Office Action at page 8 lines 6-8). A person of ordinary skill in the art in semiconductor technology is a person of ordinary creativity in the semiconductor technology. As identified in MPEP 2141.03:

> "A person of ordinary skill in the art is also a person of ordinary creativity, not an automaton." *KSR International Co. v. Teleflex Inc.*, 550 U.S. ___, ___, 82 USPQ2d 1385, 1397 (2007).
>
> The "hypothetical 'person having ordinary skill in the art' to which the claimed subject matter pertains would, of necessity have the capability of understanding the scientific and engineering principles applicable to the pertinent art." *Ex parte Hiyamizu*, 10 USPQ2d 1393, 1394 (Bd. Pat. App. & Inter. 1988) (The Board disagreed with the examiner's definition of one of ordinary skill in the art (a doctorate level engineer or scientist working at least 40 hours per week in

semiconductor research or development), finding that the hypothetical person is not definable by way of credentials, and that the evidence in the application did not support the conclusion that such a person would require a doctorate or equivalent knowledge in science or engineering.).

The Office improperly asserts that it would be obvious to a person having skill in the art to modify Nemati et al.'s memory cell by substituting the negative differential n/i/p diode having an n+ anode, a p-cathode, and an intrinsic region between the anode and cathode taught by Krivokapic for Nemati et al.'s negative differential resistance NPNP thyristor device (Final Office Action, at page 20 lines 8-12, page 18 lines 9-14).

All NDR devices are not created equally; therefore it is not proper to assert "substitution" as a rationale for combining the references.. Nemati et al. indicates that there are a variety of NDR devices. These devices have different characteristics. A quantum effect device has a different characteristic than a thyristor. Current flow through a resonant tunneling device is different than through a thyristor.

The Office has not established that the function of the NDR thyristor (which have high current density -- col. 2 lines 12-14) of Nemati et al. is the same as the function of the <u>resonant tunneling</u> diode (RTD) latch (two RTDs in series) of Krivokapic, or even the same as the function of a single RTD. A resonant tunneling current (Krivokapic) would not be considered to be a high current density for a power switch (Nemati et al.).

The Office has not established that a resonant tunneling current from an RTD would be suitable for substitution with the high current density thyristor for use in Nemati et al.'s memory cell design. One of ordinary skill in the art would not believe that this is a simple substitution.

The memory cell, as recited in the present claims, stores a charge indicative of a memory state on a floating node. The intrinsic region has an appropriate geometry to allow this storage (e.g. page 8 lines 12-14) An RTD allows 100% transmission at predetermined energy levels.

Thus, one of ordinary skill would not believe that an RTD could be simply substituted for the thyristor in the memory cell of Nemati et al.

The Office improperly dismisses proper functional language in the claims (Final Office Action, page 16 lines 1 to page 18 line 8).

The Office relies on an assertion that "a comparison of Applicant's specification to Krivokapic's disclosure reveals that Krivokapic discloses a diode that is apparently identical to the diode Applicant describes as being capable of performing the functions(s) of using the geometry of intrinsic region of the diode for assisting with stabilizing the memory state of the memory cell and allowing the memory cell to switch memory states using a forward or reverse bias voltage across the diode with gating the diode" (Final Office Action, at page 17 line 18 to page 18 line 4). This is incorrect. The geometry of the intrinsic region in the present application is capable of holding charge and is capable of providing high current (see, for example, page 8 lines 12-13, page 8 line 27 to page 9 line 4, page 11 lines 4-17, page 18 line 1 to page 20 line 16, and page 22 line 28 to page 24 line 15). There is a different structure (e.g. geometry of the intrinsic region) between the diode of the present application and the RTD of Krivokapic, and this different structure results in different functions. The RTD of Krivokapic allows for resonant tunneling (100% transmission coefficient when the incident electron has an energy that exactly equal one of the discrete energy levels inside the well). The intrinsic region in the diode in the present claims allows the claimed memory cell to hold charge.

The Office makes an improper inference when asserting that Krivokapic discloses that the substituted components and their functions were known in the art (page 19 lines 9-17).

An RTD is known. However, substituting an RTD for a thyristor, particularly in a memory circuit illustrated in Nemati et al., is not known.

The Office has not shown why one would gate a resonant tunneling diode with a diode gate.

Various claims (e.g. claim 6) recite that the diode includes a diode gate. The Office points to Nemati et al. (see, for example, page 11 lines 3-6 for this function). However, the Office asserts that one would substitute a resonant tunneling diode for the thyristor in Nemati et al., and the Office fails to identify why one would gate a resonant tunneling diode.

Thus, the Office's §103 rejection is improper for mischaracterizing the level of skill and creativity for a person of ordinary skill in the art, for dismissing functional language in the claims when such functional language is a result of the device structure, and for relying on cursory statements in an effort to support the substitution of a resonant tunneling diode for the thyristor in the memory cell of Nemati et al.

Independent Claim 1

The cited portions of Nemati et al. and Krivokapic, in conjunction with the rationale for the rejection contained in the Final Office action, do not provide the rational underpinning required to support the legal conclusion of obviousness. The Office has not established a rationale, sufficient to support the assertion that it would be obvious to substitute a RTD of Krivokapic for the thyristor in Nemati et al. for use in conjunction with the access transistor and reference voltage (V_{REF}) in Nemati et al. Further, the Office has not shown that the RTD would be able to hold a charge on the floating node in the memory cell of Nemati et al.

The Office has not provided a *prima facie* case that it would be obvious to modify Nemati et al. with an RTD to provide a memory cell that comprises an access transistor having a floating node and a diode exhibiting Negative Differential Resistance (NDR) behavior connected between the floating node and a diode reference potential line, as recited in claim 1. The diode includes an intrinsic region to assist with stabilizing the memory state of the memory cell, and the diode has a structure to allow the memory cell to switch memory states using a forward or reverse bias voltage across the diode without gating the diode. For reasons identified above, it is respectfully asserted that the RTD of Krivokapic does not have a structure capable of performing this function.

Independent Claim 6

The cited portions of Nemati et al. and Krivokapic, in conjunction with the rationale for the rejection contained in the Final Office action, do not provide the rational underpinning required to support the legal conclusion of obviousness. The Office has not established a rationale, sufficient to support the assertion that it would be obvious to substitute a RTD of Krivokapic for the thyristor in Nemati et al. for use in conjunction with the access transistor and

reference voltage (V_{REF}) in Nemati et al. Further, the Office has not shown that the RTD, with an would be able to hold a charge on the floating node in the memory cell of Nemati et al.

The Office has not provided a *prima facie* case that it would be obvious to modify Nemati et al. with an RTD to provide a memory cell that comprises an access transistor and a NDR diode, as recited in claim 6. The diode includes an anode, a cathode, an intrinsic region between the anode and cathode to assist with stabilizing the memory state of the memory cell, and a diode gate operatively positioned with respect to the intrinsic region to enhance switching performance between memory states. The RTD in Krivokapic does not have a diode gate, and the Office has not provided a rationale why one of ordinary skill would put a diode gate on a <u>resonant tunneling</u> diode (RTD). The diode has a structure to allow the memory cell to switch memory states using a forward or reverse bias voltage across the diode without gating the diode and the memory cell is adapted to gate the gate-controlled diode to enhance switching between memory states. For reasons identified above, it is respectfully asserted that the RTD of Krivokapic does not have a structure capable of performing this function.

<u>Independent Claim 7</u>

The cited portions of Nemati et al. and Krivokapic, in conjunction with the rationale for the rejection contained in the Final Office action, do not provide the rational underpinning required to support the legal conclusion of obviousness. The Office has not established a rationale, sufficient to support the assertion that it would be obvious to substitute a RTD of Krivokapic for the thyristor in Nemati et al. for use in conjunction with the access transistor and reference voltage (V_{REF}) in Nemati et al. Further, the Office has not shown that the RTD, with an would be able to hold a charge on the floating node in the memory cell of Nemati et al.

The Office has not provided a *prima facie* case that it would be obvious to modify Nemati et al. with an RTD to provide a memory cell that comprises an access transistor and a Negative Differential Resistance (NDR) n/i/p diode having an n-type anode connected to a diode reference potential line, a p-type cathode in contact with the second n-type diffusion region, and an intrinsic region between the anode and the cathode to assist with stabilizing the memory state of the memory cell, as recited in claim 7. The diode has a structure to allow the memory cell to switch memory states using a forward or reverse bias voltage across the diode without gating the

diode. For reasons identified above, it is respectfully asserted that the RTD of Krivokapic does not have a structure capable of performing this function.

Independent Claim 20

The cited portions of Nemati et al. and Krivokapic, in conjunction with the rationale for the rejection contained in the Final Office action, do not provide the rational underpinning required to support the legal conclusion of obviousness. The Office has not established a rationale, sufficient to support the assertion that it would be obvious to substitute a RTD of Krivokapic for the thyristor in Nemati et al. for use in conjunction with the access transistor and reference voltage (V_{REF}) in Nemati et al. Further, the Office has not shown that the RTD, with an would be able to hold a charge on the floating node in the memory cell of Nemati et al.

The Office has not provided a *prima facie* case that it would be obvious to modify Nemati et al. with an RTD to provide a memory cell that comprises an access transistor and a Negative Differential Resistance (NDR) diode, including an anode, a cathode, and an intrinsic region between the anode and the cathode, the diode being connected between the second diffusion region and a diode reference potential line. The diode has a structure to allow the memory cell to switch memory states using a forward or reverse bias voltage across the diode without gating the diode, and the memory cell is operative to store and sense a charge in the second diffusion region that is representative of a memory state. For reasons identified above, it is respectfully asserted that the RTD of Krivokapic does not have a structure capable of performing this function.

Independent Claim 33

The cited portions of Nemati et al. and Krivokapic, in conjunction with the rationale for the rejection contained in the Final Office action, do not provide the rational underpinning required to support the legal conclusion of obviousness. The Office has not established a rationale, sufficient to support the assertion that it would be obvious to substitute a RTD of Krivokapic for the thyristor in Nemati et al. for use in conjunction with the access transistor and reference voltage (V_{REF}) in Nemati et al. Further, the Office has not shown that the RTD, with an would be able to hold a charge on the floating node in the memory cell of Nemati et al.

The Office has not provided a *prima facie* case that it would be obvious to modify Nemati et al. with an RTD to provide a memory cell that comprises an access transistor and a gate-controlled Negative Differential Resistance (NDR) diode connected between a reference potential line and the second diffusion region as recited in claim 33. The diode includes an anode, a cathode, an intrinsic region positioned between the anode and the cathode, and a diode gate operably positioned with respect to the intrinsic region, the diode gate being connected to a second word line. The diode has a structure to allow the memory cell to switch memory states using a forward or reverse bias voltage across the diode without gating the diode and the memory cell is adapted to gate the gate-controlled diode to enhance switching between memory states. The RTD in Krivokapic does not have a diode gate, and the Office has not provided a rationale why one of ordinary skill would put a diode gate on a resonant tunneling diode (RTD).
For reasons identified above, it is respectfully asserted that the RTD of Krivokapic does not have a structure capable of performing the function.

Independent Claim 63

The cited portions of Nemati et al. and Krivokapic, in conjunction with the rationale for the rejection contained in the Final Office action, do not provide the rational underpinning required to support the legal conclusion of obviousness. The Office has not established a rationale, sufficient to support the assertion that it would be obvious to substitute a RTD of Krivokapic for the thyristor in Nemati et al. for use in conjunction with the access transistor and

reference voltage (V_{REF}) in Nemati et al. Further, the Office has not shown that the RTD, with an would be able to hold a charge on the floating node in the memory cell of Nemati et al.

The Office has not provided a *prima facie* case that it would be obvious to modify Nemati et al. with an RTD to provide a memory cell that comprises an access transistor and a Negative Differential Resistance (NDR) n/i/p diode connected between a diode reference potential line and the second diffusion region, as recited in claim 63. The n/i/p diode includes an intrinsic region positioned between the anode and the cathode. The diode has a structure to allow the memory cell to switch memory states using a forward or reverse bias voltage across the diode without gating the diode. For reasons identified above, it is respectfully asserted that the RTD of Krivokapic does not have a structure capable of performing the function.

<u>Independent Claim 72</u>

The cited portions of Nemati et al. and Krivokapic, in conjunction with the rationale for the rejection contained in the Final Office action, do not provide the rational underpinning required to support the legal conclusion of obviousness. The Office has not established a rationale, sufficient to support the assertion that it would be obvious to substitute a RTD of Krivokapic for the thyristor in Nemati et al. for use in conjunction with the access transistor and reference voltage (V_{REF}) in Nemati et al. Further, the Office has not shown that the RTD, with an would be able to hold a charge on the floating node in the memory cell of Nemati et al.

The Office has not provided a *prima facie* case that it would be obvious to modify Nemati et al. with an RTD to provide a memory device comprising a memory array with a plurality of memory cells, word lines, bits lines, at least one reference line and control circuitry, as recited in the claim. Each memory cell includes an access transistor and a NDR diode with an intrinsic region between the anode and the cathode. The diode is connected between the second diffusion region of the transistor and a diode reference line. The diode has a structure to allow the memory cell to switch memory states using a forward or reverse bias voltage across the diode without gating the diode. The memory cell is adapted to store a charge in the second diffusion region of the access transistor to indicate a stable memory state. For reasons identified above, it

is respectfully asserted that the RTD of Krivokapic does not have a structure capable of performing the function in the recited memory device.

SUMMARY

The pending claims subject to this appeal are believed patentable. Appellant respectfully submits the claims are in condition for allowance and requests the Board issue an order to withdraw the rejection of claims 1-4, 6, 7, 20, 21, 25, 26, 32-34, 37, 39, 63-65, 67, 69, 71-74 and 77.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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Date 5-12-09 By

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: MS Appeal Brief – Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 12th day of May, 2009.

Ryan Saunders

Name

Signature

8. CLAIMS APPENDIX

1. A memory cell, comprising:

an access transistor having a floating node, the floating node to store a charge indicative of a memory state of the memory cell; and

a diode exhibiting Negative Differential Resistance (NDR) behavior connected between the floating node and a diode reference potential line, the diode including an anode, a cathode and an intrinsic region between the anode and the cathode, the intrinsic region of the diode to assist with stabilizing the memory state of the memory cell, wherein the diode has a structure to allow the memory cell to switch memory states using a forward or reverse bias voltage across the diode without gating the diode.

2. The memory cell of clam 1, wherein the cathode of the diode is connected to the floating node of the access transistor.

3. The memory cell of claim 1, wherein the diode is a gate-controlled diode, and the memory cell is adapted to gate the gate-controlled diode to enhance switching between memory states.

4. The memory cell of claim 1, wherein the access transistor is formed in a bulk semiconductor structure.

6. A memory cell, comprising:

an access transistor having a first diffusion region connected to a bit line, and a second diffusion region, the second diffusion region to store a charge indicative of a memory state of the memory cell;

a Negative Differential Resistance (NDR) diode connected between the second diffusion region and a diode reference potential line, the diode including: an anode; a cathode; an intrinsic region between the anode and cathode to assist with stabilizing the memory state of the memory

cell; and a diode gate operatively positioned with respect to the intrinsic region to enhance switching performance between memory states, wherein the diode has a structure to allow the memory cell to switch memory states using a forward or reverse bias voltage across the diode without gating the diode and the memory cell is adapted to gate the gate-controlled diode to enhance switching between memory states.

7. A memory cell, comprising:

an n-channel access transistor on a bulk semiconductor substrate, the n-channel access transistor having a first n-type diffusion region connected to a bit line and a second n-type diffusion region, the second n-type diffusion region to store a charge indicative of a memory state of the memory cell; and

a Negative Differential Resistance (NDR) n/i/p diode having an n-type anode connected to a diode reference potential line, a p-type cathode in contact with the second n-type diffusion region, and an intrinsic region between the anode and the cathode to assist with stabilizing the memory state of the memory cell, wherein the diode has a structure to allow the memory cell to switch memory states using a forward or reverse bias voltage across the diode without gating the diode.

20. A memory cell, comprising:

an access transistor, including:

a body region;

a first diffusion region electrically connected to a bit line;

a second diffusion region separated from the first diffusion region by a channel area in the body region;

a gate separated from the channel area by a gate insulator, the gate electrically connected to a word line;

a Negative Differential Resistance (NDR) diode, including an anode, a cathode, and an intrinsic region between the anode and the cathode, the diode being connected between the second diffusion region and a diode reference potential line, wherein the diode has a structure to

allow the memory cell to switch memory states using a forward or reverse bias voltage across the diode without gating the diode,

wherein the memory cell is operative to store and sense a charge in the second diffusion region that is representative of a memory state.

21. The memory cell of claim 20, wherein the access transistor includes an n-channel transistor.

25. The memory cell of claim 20, wherein the diode includes an n/i/p diode having an n-type anode, a p-type cathode, and an intrinsic region between the anode and cathode.

26. The memory cell of claim 25, wherein the n/i/p diode includes an n+/i/p diode having an n+ anode, a p cathode, and an intrinsic region between the anode and cathode.

32. The memory cell of claim 20, wherein the access transistor is on a bulk semiconductor substrate.

33. A memory cell, comprising:

an access transistor formed in a bulk semiconductor structure, the access transistor including a first diffusion region separated from a second diffusion region by a channel region, and further including a gate separated from the channel region by a gate insulator, wherein the first diffusion region is connected to a bit line and the gate is connected to a first word line; and

a gate-controlled Negative Differential Resistance (NDR) diode connected between a reference potential line and the second diffusion region, the diode including an anode, a cathode, an intrinsic region positioned between the anode and the cathode, and a diode gate operably positioned with respect to the intrinsic region, the diode gate being connected to a second word line,

wherein the diode has a structure to allow the memory cell to switch memory states using a forward or reverse bias voltage across the diode without gating the diode and the memory cell is adapted to gate the gate-controlled diode to enhance switching between memory states.

34. The memory cell of claim 33, wherein the diode is formed such that the intrinsic region has a desired geometry to assist with stabilizing the memory state of the memory cell.

37. The memory cell of claim 33, wherein the gate-controlled diode includes a vertically-oriented diode.

39. The memory cell of claim 33, wherein:

the first and second diffusion regions of the access transistor include n-type dopants; and

the gate-controlled diode includes an n/i/p diode having an n-type anode connected to the reference potential line and a p-type cathode in contact with the second diffusion region.

63. A memory cell, comprising:

an access transistor, including a first diffusion region separated from a second diffusion region by a channel region, and further including a gate separated from the channel region by a gate insulator, wherein the first diffusion region is connected to a bit line and the gate is connected to a first word line; and

a Negative Differential Resistance (NDR) n/i/p diode connected between a diode reference potential line and the second diffusion region, the n/i/p diode including an n-type anode, a p-type cathode, and an intrinsic region positioned between the anode and the cathode, wherein the diode has a structure to allow the memory cell to switch memory states using a forward or reverse bias voltage across the diode without gating the diode.

64. The memory cell of claim 63, wherein the n/i/p diode includes an n+/i/p diode, including an n+ anode, a p cathode, and an intrinsic region positioned between the anode and the cathode.

65. The memory cell of claim 63, wherein the diode includes a gate-controlled diode having a diode gate operably positioned with respect to the intrinsic region, the diode gate being connected to a second word line.

67. The memory cell of claim 63, wherein the access transistor and the diode are on a bulk semiconductor substrate.

69. The memory cell of claim 63, wherein the diode includes a vertically-oriented diode.

71. The memory cell of claim 63, wherein the access transistor includes an n-channel transistor.

72. A memory device, comprising:

a memory array, including a plurality of memory cells in rows and columns;

a number of word lines, each word line connected to a row of memory cells;

a number of bit lines, each bit line connected to a column of memory cells;

at least one reference line to provide a reference potential to the memory cells;

control circuitry, including word line select circuitry and bit line select circuitry to select a number of memory cells for writing and reading operations,

wherein each memory cell includes:

an access transistor, including a body region, a first diffusion region electrically connected to one of the bit lines, a second diffusion region separated from the first diffusion region by a channel area in the body region, and a gate separated from the channel area by a gate insulator and electrically connected to one of the word lines; and

a Negative Differential Resistance (NDR) diode, including an anode, a cathode, and an intrinsic region between the anode and the cathode, the diode being connected between the second diffusion region and a diode reference line, wherein the diode has a structure to allow the memory cell to switch memory states using a forward or reverse bias voltage across the diode without gating the diode,

wherein the memory cell is adapted to store a charge in the second diffusion region of the access transistor to indicate a stable memory state.

73. The memory device of claim 72, wherein the diode includes a gate-controlled diode, and the memory device is adapted to gate the gate-controlled diode to enhance switching between memory states.

74. The memory device of claim 72, wherein each memory cell is on a bulk semiconductor substrate, and the diode includes a vertically-oriented diode.

77. The memory device of claim 76, wherein the vertical-oriented diode is at least partially formed in the floating body of the access transistor.

9. EVIDENCE APPENDIX

None.

10. RELATED PROCEEDINGS APPENDIX

None.